a memory circuit for coupling said local memory of said first processor to said local memory of said second processor.

7. The apparatus of Claim 6, wherein said first processor is the main processor of said apparatus.

8. The apparatus of Claim 7, wherein said first processor is a microprocessor.

9. The apparatus of Claim 7, wherein said first processor is a digital signal processor "DSP".

10. The apparatus of Claim 6, wherein said program memory of said first processor is ROM memory.

11. The apparatus of Claim 6, wherein said local memory of said first processor is RAM memory.

12. The apparatus of Claim 6, wherein said local memory of said second processor is ROM memory.

13. The apparatus of Claim 6, wherein said local memory of said second processor is RAM memory.

14. The apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is physically separate from said first and second processors.

15. The apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is a DPRAM memory.

16. The apparatus of Claim 6, wherein said second processor is a protocol processor.

17. The apparatus of Claim 6, wherein said synchronizing circuit ensures that only one of said first and processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time.

18. The apparatus of Claim 6, wherein said second processor comprises:

an incremental register;

a program memory connected to the incremental register;

19. The apparatus of Claim 6, wherein an instruction set is provided to said protocol processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions:

integers corresponding to arithmetic and logic operations on integer numbers;

transfer corresponding to the transfer operations between a register in said protocol processor and memory;

monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said protocol processor.

20. An apparatus, comprising:

a first processor core;

a first program memory coupled to said first processor core;

a first local memory coupled to said first processor core;

a second processor core;

a second program memory coupled to said second processor core;

a second local memory coupled to said second processor core;

a synchronizing circuit coupling said first processor core to said second processor core; and

a memory circuit coupling said first local memory to said second local memory.

21. The apparatus of Claim 20, wherein said first processor core, said first program memory and said first local memory comprise a processor.

22. The apparatus of Claim 20, wherein said first processor core, said first program memory, said first local memory and said memory circuit comprise a processor.

23. The apparatus of Claim 20, wherein said second processor core, said second program memory and said second local memory comprise a processor.

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24. The apparatus of Claim 20, wherein said first processor core, said first program memory and said first local memory comprise a first processor and said second processor core, said second program memory and said second local memory comprise a second processor.

25. The apparatus of Claim 20, wherein said first processor core, said first program memory, said first local memory and said memory circuit comprise a first processor and said second processor core, said second program memory and said second local memory comprise a second processor.

26. A cellular radio, comprising:

a first processor;

a second processor coupled to said first processor; and

a third processor coupled to said first processor.

27. The cellular radio of Claim 26, wherein said first processor is the main processor of the cellular radio.

28. The cellular radio of Claim 26, wherein said first processor performs management and vocoder signal processing.

29. The cellular radio of Claim 26, wherein said second processor performs protocol processing.

30. The cellular radio of Claim 29, wherein said second processor is a dedicated processor adapted to bit processing.

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31. The cellular radio of Claim 26, wherein said third processor performs signal processing on vectors.

32. The cellular radio of Claim 31, wherein said third processor is a dedicated processor of the array processor type.

33. The cellular radio of Claim 26, wherein said first, second and third processors operate in parallel.

Claims 6-33 stand allowable over the cited art and the application is in allowable form. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,

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